Invited Journal Articles

1. H.-Y. Chen, S. Brivio, C.-C. Chang, J. Frascaroli, H.-H. Hou, B. Hudec, M. Liu, H. Lv, G. Molas, J. Sohn, S. Spiga, V.M. Teja, E. Vianello, H.-S. P. Wong, "Resistive random access memory (RRAM) technology: From material, device, selector, 3D integration to bottom-up fabrication," invited paper, *J. Electroceramics*, 24 June, 2017. DOI 10.1007/s10832-017-0095-9
2. H.-S. P. Wong and S. Salahuddin, "Memory Leads the Way to Better Computing," invited paper, *Nature Nanotechnology*, Vol. 10, pp. 191 – 194 (2015). doi:10.1038/nnano.2015.29
3. S. Hong, S.H. Chang, C. Phatak, B. Magyari-Köpe, Y. Nishi, S. Chattopadhyay, J.H. Kim, "Mechanism study of reversible resistivity change in oxide thin film", ECS Trans. 69, 52, 2015.
4. M. Caldwell, R.G.D. Jeyasingh, H.-S. P. Wong, D. Milliron, "Nanoscale Phase Change Memory Materials," invited feature article *Nanoscale*, vol. 4, pp. 4382 – 4392 (2012). DOI: 10.1039/C2NR30541K
5. H.-S. P. Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen, B. Lee, F.T. Chen, M.-J. Tsai, "Metal Oxide RRAM," invited paper, *Proceedings of the IEEE*, vol. 100, No. 6, pp. 1951 – 1970, June, 2012.

Refereed Journal Articles

1. H. Li, P. Huang, B. Gao, X. Liu, J. Kang, and H.-S. P. Wong, "Device and Circuit Interaction Analysis of Stochastic Behaviors in Cross-Point RRAM Arrays," *IEEE Transactions on Electron Devices, 64*(12), pp.4928 – 4936, 2017.
2. S.W. Fong, C.M. Neumann, and H.-S. P. Wong, "Phase-Change Memory – Toward a Storage-Class Memory," *IEEE Trans. Electron Devices*, Volume: 64, Issue: 11, pp. 4374 – 4385 (2017). DOI: 10.1109/TED.2017.2746342
3. S. W. Fong, C.M. Neumann, E. Yalon, M.M. Rojo, E. Pop, H.-S.P. Wong, "Dual-Layer Dielectric Stack for Thermally Isolated Low-Energy Phase-Change Memory," *IEEE Transactions on Electron Devices, 64*(11), pp.4496 – 4502, 2017
4. *F. Yuan*, Z. Zhang, C. Liu, F. Zhou, H.M. Yao, W. Lu, X. Qiu, H.-S. P. Wong, J. Dai, and Y. Chai, "Real-time observation of the electrode-size-dependent evolution dynamics of the conducting filaments in a SiO2 layer. *ACS Nano*, 11(4), pp.4097 – 4104, 2017
5. J.-C. Liu, B. Magyari-Kope, S. Qin, X. Zheng, H.-S. P. Wong, T.-H. Hou, "AC Stress and Electronic Effects on SET Switching of HfO_2 RRAM," *Appl. Phys. Lett*. 111, 093502 (2017). doi: 10.1063/1.4991576
6. M.M. Shulaker, G. Hills, R. S. Park, R.T. Howe, K. Saraswat, H.-S. P. Wong, S. Mitra, "Three-dimensional Integration of Nanotechnologies for Computing and Data Storage on a Single Chip," Nature, Vol. 547, pp. 74 – 78, 2017. doi:10.1038/nature22994

7. Z. Wang, Z. Jiang, X. Zheng, S. Fong, H.-Y. Chen, H.-S. P. Wong, Y. Nishi, “Ultrafast Accelerated Retention Test Methodology for RRAM Using Micro Thermal Stage,” *IEEE Electron Device Letters*, vol. 38, no. 7, pp. 863-866, July 2017. doi: 10.1109/LED.2017.2700398
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9. E. Yalon, S. Deshmukh, M. Muñoz Rojo, F. Lian, C.M. Neumann, F. Xiong, E. Pop, "Spatially Resolved Thermometry of Resistive Memory Devices," *Scientific Reports* 7, 15360 (2017).
10. L. Gao, E. Yalon, A.R. Chew, S. Deshmukh, A. Salleo, E. Pop, A.A. Demkov, "Effect of oxygen vacancies and strain on the phonon spectrum of HfO_2," *J. Appl. Phys.* 121, 224101 (2017).
11. Kumar, S., Wang, Z., Davila, N., Kumari, N., Norris, K.J., Huang, X., Strachan, J.P., Vine, D., Kilcoyne, A.D., Nishi, Y. and Williams, R.S., “Physical origins of current and temperature controlled negative differential resistances in NbO2”. Nature communications, 2017, 8(1), p.658.
12. Kumar, S., Wang, Z., Huang, X., Kumari, N., Davila, N., Strachan, J.P., Vine, D., Kilcoyne, A.D., Nishi, Y. and Williams, R.S., “Oxygen migration during resistance switching and failure of hafnium oxide memristors”. Applied Physics Letters, 2017, 110(10), p.103503.
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15. D. Duncan, B. Magyari Kope and Y. Nishi, ”Properties of Dopants in HfOx for Improving the Performance of Nonvolatile Memory” Phys. Rev. Applied, 7, 034020, 2017
16. K. Jung, B. Magyari Kope and Y. Nishi, “Hydrogen-Induced Oxygen Vacancy Bistable and its Impact on RRAM Device Operation, IEEE Electron Devices Lett., 2017
17. L. Zhao, B.Magyari Kope and Y. Nishi, “Polaronic Interactions between Oxygen vacancies in Rutile TiO2”, Phys. Rev. B95, 054104, 2017
18. Kumar, S., Wang, Z., Huang, X., Kumari, N., Davila, N., Strachan, J.P., Vine, D., Kilcoyne, A.D., Nishi, Y. and Williams, R.S., “Conduction channel formation and dissolution due to oxygen thermophoresis/diffusion in hafnium oxide memristors”. ACS nano, 2016, 10(12), pp.11205-11210.

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27. M.M. Sabry Aly, M. Gao, G. Hills, C.-S. Lee, G. Pitner, M.M. Shulaker, T.F. Wu, M. Asheghi, J. Bokor, F. Franchetti, K.E. Goodson, C. Kozyrakis, I. Markov, K. Olukotun, L. Pileggi, E. Pop, J. Rabaey, C. Re, H.-S. P. Wong, S. Mitra, "Energy-Efficient Abundant-Data Computing: The N3XT 1,000X," *IEEE Computer*, pp. 24 – 33, December 2015.

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29. *S. Lee*†, J. Sohn†, Z. Jiang, H.-Y. Chen, H.-S. P. Wong, "Metal Oxide-Resistive Memory using Graphene-edge Electrodes," Nature Communications, 6, Article 8407, September 25, 2015. †=equal contribution. doi:10.1038/ncomms9407

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Resistive Random Access Memory," *Nanotechnology*, 24, 465201, 2013. doi:10.1088/0957-4484/24/46/465201

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Invited Conference Presentations

1. H.-S. P. Wong, "Reaching for the N3XT 1,000× of Computing Energy Efficiency," invited plenary paper, *Semiconductor Integrated Circuit Technology Workshop (SICTW) at West Lake*, Zhejiang University, Hangzhou, China, November 6 – 9, 2017
2. E. Pop, "Fundamental, Thermal, and Energy Limits of PCM and ReRAM", Tutorial at *Intl. Electron Devices Meeting (IEDM)*, San Francisco, CA, Dec 2017.
3. E. Yalon and E. Pop, "Spatially Resolved Thermometry of PCM Devices", *IEEE Non-Volatile Memory Technol. Symp. (NVMTS)*, Aug. 2017.
4. E. Pop, "Fundamentals and Ultimate Scaling Limits of Phase-Change Memory," Tutorial at *75th Device Research Conference (DRC)*, Notre Dame, IN, Jun 2017.

5. H.-S. P. Wong, "The N3XT 1,000× of Computing Energy Efficiency," invited keynote paper, *1st International Semiconductor Conference for Global Challenges (ISCGC)*, Nanjing, China, July 17 – 19, 2017.
6. H.-S. P. Wong, "Resistive Switching Memory," ChinaRRAM Workshop, Suzhou, China, June 12 – 13, 2017.
7. H.-S. P. Wong, "The N3XT 1,000× of Computing Energy Efficiency," invited paper, *Materials Research Society (MRS) Spring Meeting*, Advanced Interconnects for Logic and Memory Applications—Materials, Processes and Integration, Phoenix, AZ, April 17 – 21, 2017.
8. H. Li, T. F. Wu, S. Mitra, H.-S. P. Wong, "Device-Architecture Co-Design for Hyperdimensional Computing with 3D Vertical Resistive Switching Random Access Memory (3D VRRAM)," invited paper, *International Symposium on VLSI Technology, Systems and Applications (2017 VLSI-TSA)*, Hsinchu, Taiwan, 24- 27 April, 2017.
9. S. W. Fong, C. M. Neumann, and H.-S. P. Wong, "Phase-change Memory – Towards a Storage Class Memory"," invited plenary talk, *International Symposium on Non-Volatile Memory*, Hsinchu, Taiwan, March 27, 2017.
10. H.-S. P. Wong, "Memory – the N3XT Frontier," invited keynote paper, 8th Annual Non-Volatile Memories Workshop (NVMW 2017), La Jolla, CA March 12-14, 2017
11. F. Xiong, E. Yalon, A. Behnam, C.M. Neumann, K.L. Grosse, S. Deshmukh, and E. Pop, "Towards Ultimate Scaling Limits of Phase-Change Memory", *IEEE Int. Elec. Dev. Meeting (IEDM)*, Dec. 2016.
12. H.-S. P. Wong, "Computing Performance: The N3XT 1,000X," invited talk, *JSPS165 International Symposium on Device Technology for Next-Generation Computing*, University of Tokyo, Tokyo, Japan. September 30, 2016.
13. H.-S. P. Wong, "Memory, the N3XT Frontier," invited plenary talk, IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC'16), Hong Kong, August 3 – 5, 2016.
14. H.-S. P. Wong, "Device Technologies for the N3XT 1,000X Improvement in Computing Performance," keynote speaker, Architecture 2030 Workshop @ ISCA 2016, Seoul, Korea, June 19, 2016.
15. Yoshio Nishi, "Recent progress in physics and technology of oxide based resistive switching memory", IEEE Silicon Valley Nanoelectronics Workshop, June, 2015, Santa Clara, CA
16. Y. Nishi, "Emerging Nonvolatile Memory Devices ", JSPS anniversary international workshop, November 5, 2015, Univ. Tokyo, Japan
17. H.-S. P. Wong, "Computing Performance: The N3XT 1,000X," invited talk, *IEEE Rebooting Computing Summit 4 (RCS4)*, Washington, DC, December 10 – 11, 2015.
18. H.-S. P. Wong, "Memory Leads the Way to Better Computing: the N3XT 1,000X in Energy Efficiency," *Design Automation Conference (DAC)*, San Francisco, June 7 –

11, 2015. Invited paper in *Session 2W, "Workshop 2: Design Automation for Beyond-CMOS Technologies"*

19. M. S. Ebrahimi, G. Hills, M. M. Sabry, M. M. Shulaker, H. Wei, T. F. Wu, S. Mitra, H.-S. P. Wong, "Monolithic 3D Integration Advances and Challenges: From Technology to System Levels", invited paper, IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), Millbrae, CA, October 6 – 10, 2014.
20. H.-Y. Chen, M. Shulaker, S. Yu, H. Wei, B. Gao, J. Kang, S. Mitra, and H.-S. P. Wong, "Monolithic 3D Integration of Logic and Memory," invited paper, 16th ACM/IEEE System Level Interconnect Prediction (SLIP), San Francisco, CA, June 1, 2014.
21. J.F. Kang, B.Gao, Y.J. Bi, B. Chen, and X.Y. Liu, S.M. Yu, H-Y. Chen, and H.-S. P. Wong, "TMO-based Memristive Devices and Application for Neuromorphic Systems," invited paper, *13th International Conference on Modern Materials and Technologies* (CIMTEC), 6th Forum on New Materials, Montecantini Terme, Italy, June 15 – 20, 2014.
22. J.F. Kang, B. Gao, B. Chen, P. Huang, F.F. Zhang, X.Y. Liu, H-Y. Chen, Z. Jiang, H.-S. P. Wong, S.M. Yu, "Scaling and Operation Characteristics of HfOx Based Vertical RRAM for Cost-Effective 3D Cross-Point Architecture," invited paper, IEEE Symposium on Circuits and Systems (*ISCAS*), Melbourne, Australia, June 1 – 5, 2014.
23. S. Yu, Y. Deng, B. Gao, P. Huang, B. Chen, X. Y. Liu, J. F. Kang, H.-Y. Chen, Z. Jiang, and H.-S. P. Wong, "Design guidelines for 3D RRAM cross-point architecture," invited paper, IEEE Symposium on Circuits and Systems (*ISCAS*), Melbourne, Australia, June 1 – 5, 2014.
24. S. Yu, Y. Wu, H-Y. Chen, Z. Jiang, J. Sohn, H.-S. P. Wong, "Metal–Oxide-Based Resistive Switching Memory (RRAM): Modeling, Scaling, and 3D integration," invited paper, *Materials Research Society Spring Meeting* (MRS), paper BB10.02, April 21 – 25, 2014.
25. Blanka Magyari-Köpe, Yoshio Nishi, "Modeling the Resistive Switching Process in Transition Metal Oxide Based Non-Volatile Memory Devices", 16th International Workshop on Computational Electronics (IWCE), Nara, Japan, June 2013
26. Blanka Magyari-Kope and Y. Nishi, "Modeling aspects of forming and switching in RRAM devices, including possible doping effects forimproved characteristics", NCCAVS Thin Film Users Group (TFUG) "Advanced Memory Meeting", November 2013, San Jose, USA
27. B. Magyari-Kope and Y. Nishi, "Ab initio calculations for RRAM devices," 3rd International Workshop on Resistive Memories, IMEC, October 2013, Leuven, Belgium.
28. B. Magyari-Kope and Y. Nishi, "Binary transition metal oxides for resistive memory applications", October 2013.International CECAM-Workshop "Functional Oxides for Emerging Technologies", Bremen, Germany

29. S. Yu, *X. Guan*, Y. Wu, H.-S. P. Wong, "Characterization and Modeling of the Conduction and Switching Mechanism of HfOx based RRAM," invited paper, *MRS Fall 2013 Symposium on "Emergent Electron Transport Properties at Complex Oxide Interfaces",* Boston, MA, 2013.
30. H.-S. P. Wong, "3D RRAM," invited paper, New Non-Volatile Memory Workshop, Hsinchu, Taiwan, November 14, 2013.
31. H. Yi, Y. Wu, Z. Zhang, H.-Y. Chen, S. Yu, H.-S. P. Wong, "Metal Oxide Resistive Switching Memory (RRAM): Devices, Fabrication, and Self-Assembly Patterning for Random Logic and Memory Devices (SRAM, NAND, RRAM)," invited plenary talk, 26th International Microprocesses and Nanotechnology Conference, Hokkaido, Japan, November 5 – 8, 2013.
32. H.-S. P. Wong, "3D RRAM," invited paper, Third International Workshop on RRAM, Leuven, Belgium, October 18 – 18, 2013.
33. Y. Wu, S. Yu, H.-Y. Chen, J. Liang, Z. Jiang, H.-S. P. Wong, "Resistive Switching Random Access Memory (RRAM) – Materials, Device, Scaling, and Array Design," invited paper, *60th International Symposium of the American Vacuum Society (AVS)*, Long Beach, CA, October 27 – November 1, 2013.
34. R.G.D. Jeyasingh, S. W. Fong, J. Lee, E. Bozorg-Grayeh, C. Ahn, M. Asheghi, K.E. Goodson, and H.-S. P. Wong, "Phase Change Memory – The Interplay Between Thermal and Electrical Effects," invited paper, 224th Electrochemical Society (ECS) Meeting, Symposium E5: Non-Volatile Memories Symposium, San Francisco, CA, October 30-31, 2013.
35. H.-Y. Chen, S. Yu, Y. Wu, H.-S. P. Wong, "3D Vertical RRAM Architecture and Electrode/Oxide Interface Engineering for Next Generation Mass Storage," invited paper, International Conference on Solid State Devices and Materials (SSDM), Fukuoka, Japan, September 24-27, 2013.
36. C.-S. Lee, S. Yu, *X. Guan*, J. Luo, L. Wei, H.-S. P. Wong, "Compact Models of Emerging Devices," invited paper, IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC'13), Hong Kong, June 3 – 5, 2013.
37. H.-S. P. Wong, "Emerging Memory Devices," keynote talk, China Semiconductor Technology International Conference (CSTIC), Symposium VI: "Materials and Process Integration for Device and Interconnection," Shanghai, China, March 17 – 18, 2013.
38. Blanka Magyari-Köpe, Yoshio Nishi, "Atomic-size Effects of the Conductive Filaments Formation and Rupture in Resistance Change Based Memory Devices", International Conference on Small Science (ICSS), Orlando, USA, December 2012
39. H.-S. P. Wong, *X. Guan*, *D. Kuzum*, R. Jeyasingh, S. Yu, "Variability in Emerging Memory Devices: Physical Understanding, Modeling, and Mitigation," invited keynote paper, *IEEE Workshop on Variability Modeling and Characterization* (VMC), San Jose, CA, November 8, 2012.
40. Y. Wu, J. Liang, S. Yu, *X. Guan*, and H.-S. P. Wong, "Resistive switching random access memory - materials, device, interconnects, and scaling considerations", invited

talk, IEEE International Integrated Reliability Workshop (IIRW), October 14-18, 2012, Fallen Leaf Lake, CA, USA.

41. H.-S. P. Wong, "Emerging Memory Devices," keynote invited talk, *9th International Symposium on Advanced Gate Stack Technology*, Saratoga, New York, October 3 – 4, 2012.
42. R. Jeyasingh, J. Liang, M. A. Caldwell, *D. Kuzum*, H.-S. P. Wong, "Phase Change Memory: Scaling and Applications," invited paper, *IEEE Custom Integrated Circuits Conference* (CICC), San Jose, CA, September 9 – 12, 2012.
43. H.-S. P. Wong, "Emerging Memory Devices," invited keynote paper, *1st Asian Nonvolatile Memory Workshop*, Tsinghua University, Beijing, China, July 19 – 20, 2012.
44. *X. Guan*, S. Yu, H.-S. P. Wong, "On the Variability of HfO_x RRAM: From Numerical Simulation to Compact Modeling," invited paper, *Workshop on Compact Modeling (WCM)*, San Jose, CA, June 18 -21, 2012.
45. Y. Wu, S. Yu, *X. Guan*, H.-S. P. Wong, "Recent Progress of Resistive Switching Random Access Memory (RRAM)," invited paper, Silicon Nanoelectronics Workshop (SNW), invited paper, Honolulu, Hawaii, June 10 – 11, 2012.
46. H.-S. P. Wong, "Phase Change Memory," invited speaker, *International Symposium on Nonvolatile Memory – the Technology Driver of the Electronics Industry*, Hsinchu, Taiwan, March 26, 2012.

Contributed Conference Presentations

1. S. Deshmukh, F. Lian, E. Yalon, G. Pitner, H.-S.P. Wong, E. Pop, "Sub-15 nm Nanowires Enabled by Cryo Pulsed Self-Aligned Nanotrench Ablation on Carbon Nanotubes," *IEEE Nano*, Jul 2017, Pittsburgh PA.
2. S. Colburn, A. Zhan, A. Majumdar, S. Deshmukh, E. Pop, J. Myers, J. Frantz, "Active Metasurfaces Based on Phase-Change Memory Material Digital Metamolecules," *IEEE Nano*, Jul 2017, Pittsburgh PA.
3. S. Bohaichuk, G. Pitner, F. Lian, J. Jeong, M.G. Samant, S.S.P. Parkin, H.-S. Philip Wong, E. Pop, "Probing Metal-Insulator Transitions in VO_2 with Ultra-Narrow Carbon Nanotube Electrodes," *MRS Spring Meeting*, Apr 2017, Phoenix AZ.
4. *Y. Shi*, C. Pan, V. Chen, N. Raghavan, K.L. Pey, F.M. Puglisi, E. Pop, H.-S. P. Wong, M. Lanza, "Coexistence of volatile and non-volatile resistive switching in 2D h-BN based electronic synapses," *International Electron Devices Meeting (IEDM)*, paper 5.4, December 4 – 6, San Francisco, 2017.
5. R. Yang, H. Li, K.K.H. Smithe, T. R. Kim, K. Okabe, E. Pop, J. A. Fan, H.-S. P. Wong, "2D Molybdenum Disulfide (MoS_2) Transistors Driving RRAMs with 1T1R Configuration," *International Electron Devices Meeting (IEDM)*, paper 19.5, December 4 – 6, San Francisco, 2017.

6. *C.-W. Hsu*, X. Zheng, Y. Wu, T.-H. Hou, H.-S. P. Wong, J. Kang, "Statistical Study of RRAM MLC SET Variability Induced by Filament Morphology," *IEEE International Reliability Physics Symposium* (IRPS), Monterey, CA, April 2 – 6, 2017.
7. Z. Jiang, Z. Wang, X. Zheng, S. Fong, S. Qin, H.-Y. Chen, C. Ahn, *J. Cao*, Y. Nishi, and H.-S. P. Wong, "Microsecond Transient Thermal Behavior of HfOx-based Resistive Random Access Memory Using a Micro Thermal Stage (MTS)," *IEEE International Electron Devices Meeting (IEDM)*, paper 21.3, December 5 – 7, San Francisco, 2016.
8. H. Li, T.F. Wu, A. Rahimi. K.-S. Li, M. Rusch, C.-H. Lin, J.-L. Hsu, M.M. Sabry, S.B. Eryilmaz. J. Sohn, W.-C. Chiu, M.-C. Chen, T.-T. Wu, J.-M. Shieh, W.-K. Yeh, J. M. Rabaey, S. Mitra, and H.-S. P. Wong, "Hyperdimensional Computing with 3D VRRAM In-Memory Kernels: Device-Architecture Co-Design for Energy-Efficient, Error-Resilient Language Recognition," *IEEE International Electron Devices Meeting (IEDM)*, paper 16.1, December 5 – 7, San Francisco, 2016.
9. Pranav Ramesh, Raisul Islam, Donovan Lee, Kurt Weiner, Krishna Saraswat, "Control of Resistivity and Stoichiometry in Atomic Layer Deposited Titanium Dioxide Using Rapid Thermal Annealing," MRS Spring 2016 meeting, March 2016, Phoenix, Arizona.
10. Z. Jiang, P. Huang, L. Zhao, S. Kvatinsky, S. Yu, X. Liu, J. Kang, Y. Nishi, H.-S. P. Wong, "Performance Prediction of Large-Scale 1S1R Resistive Memory Array Using Machine Learning," *International Memory Workshop (IMW)*, Monterey, CA, May 15 – 17, 2015.
11. H. Li, Z. Jiang, P. Huang, Y. Wu, H.-Y. Chen, B. Goa, X.Y. Liu, J.F. Kang, H.-S. P. Wong, "Variation-Aware, Reliability-Emphasized Design and Optimization of RRAM Using SPICE Model," Design, Automation & Test in Europe Conference and Exhibition (*DATE*), Grenoble, France, pp. 1425 – 1430, March 9 – 13, 2015.
12. S. Deshmukh, R. Islam, C. Chen, E. Yalon, K. C. Saraswat and E. Pop, "Thermal modeling of metal oxides for highly scaled nanoscale RRAM," 2015 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Washington, DC, 2015, pp. 281-284.
13. S. Deshmukh, F. Xiong, F. Lian, Y. Cui, E. Pop, "Characterization of Highly Resistive Nanoscale RRAM Contacts," MRS Spring Meeting, Apr 2015, San Francisco CA.
14. M. Shulaker, T. Wu, A. Pal, K. Saraswat, H.-S. P. Wong, S. Mitra, "Monolithic 3D Integration of Logic and Memory: Carbon Nanotube FETs, Resistive RAM, and Silicon FETs," *IEEE International Electron Devices Meeting (IEDM)*, paper 27.4, pp. 638 – 641, December 15 – 17, San Francisco, 2014.
15. *J. H. Engel*, S. B. Eryilmaz, S. Kim, M. BrightSky, C. Lam, B. A. Olshausen, and H.-S. P. Wong, "Capacity Optimization of Emerging Memory Systems: A Shannon-Inspired Approach to Device Characterization," *IEEE International Electron Devices Meeting (IEDM)*, paper 29.4, pp. 693 – 696, December 15 – 17, San Francisco, 2014.

16. L. Zhao, Z. Jiang, H.-Y. Chen, J. Sohn, K. Okabe, B. Magyari-Köpe, H.-S. P. Wong, Y. Nishi, "Ultrathin (~2nm) HfOx as the Fundamental Resistive Switching Element: Thickness Scaling Limit, Stack Engineering and 3D Integration," *IEEE International Electron Devices Meeting (IEDM)*, paper 6.6, pp. 156 – 159, December 15 – 17, San Francisco, 2014.
17. J. Sohn, *S. Lee*, Z. Jiang, H.-Y. Chen, H.-S. P. Wong, "Atomically Thin Graphene Plane Electrode for 3D RRAM," *IEEE International Electron Devices Meeting (IEDM)*, paper 5.3, pp. 116 – 119, December 15 – 17, San Francisco, 2014.
18. Z. Jiang, S. Yu, Y. Wu, *J. H. Engel*, *X. Guan*, H.-S. P. Wong, "Verilog-A Compact Model for Oxide-based Resistive Random Access Memory (RRAM)," International Conference on Simulation of Semiconductor Processes and Devices (*SISPAD*), paper 3-3, Yokohama, Japan, September 9 – 11, 2014.
19. *J. Provine*, Z. Zhang, Z. Fang, S. Yeh, Y. Wu, J. Sohn, H. Yi, T.F. Wu, B.B. Weng, X. Wang, G.-Q. Lo, S. Mitra, H.-S. P. Wong, S. Wong, "Advances in RRAM Through Split Manufacturing and Aggressive Scaling," *39th Annual GOMACTech Conference*, pp. 93 – 97, paper 7.1, Charleston, SC, March 31 – April 3, 2014.
20. H.-Y. Chen, B. Gao, H. Li, R. Liu, P. Huang. Z. Chen, B. Chen, F. Zhang, L. Zhao, Z. Jiang, L. Liu, X. Liu J. Kang, S. Yu, Y. Nishi, H.-S. P. Wong, "Towards High-Speed, Write-Disturb Tolerant 3D Vertical RRAM Arrays," *Symp. VLSI Technology*, Honolulu, HI, paper T22.2, June 9 – 13, 2014.
21. C. Ahn, Z. Jiang, C.-S. Lee, H.-Y. Chen, J. Liang, L. S. Liyanage, and H.-S. P. Wong, "A 1TnR Array Architecture using a One-Dimensional Selection Device," *Symp. VLSI Technology*, paper T15.4, Honolulu, HI, June 9 – 13, 2014.
22. H. Li, Z. Jiang, P. Huang, H.-Y. Chen, B. Chen, R. Liu, Z. Chen, F. Zhang, L. Liu, B. Gao, X. Liu, S. Yu. H.-S. P. Wong, J. Kang, "Statistical Assessment Methodology for the Design and Optimization of Cross-Point RRAM Arrays," *International Memory Workshop (IMW)*, Taipei, Taiwan, May 18 – 21, 2014.
23. H. Li, H.Y. Chen, Z. Chen, B. Chen, R. Liu, G. Qiu, P. Huang, F. Zhang, Z. Jiang, B. Gao, L. Liu, X. Liu, S. Yu, H.-S. P. Wong, J. Kang, "Write Disturb Analyses on Half-Selected Cells of Cross-Point RRAM Arrays," *IEEE International Reliability Physics Symposium* (IRPS), paper MY-3, Waikoloa, HI, June 1 – 5, 2014.
24. A. Sood, S. B. Eryilmaz, R. Jeyasingh, J. Cho, M. Asheghi, H.-S. P. Wong, and K. E. Goodson, "Thermal characterization of nanostructured superlattices of TiN/TaN: Applications as electrodes in Phase Change Memory," IEEE ITHERM Conference, pp. 765 – 770, Orlando, FL, May 27 – 30, 2014, DOI: 10.1109/ITHERM.2014.6892358
25. S. Fong, R. Jeyasingh, M. Asheghi, K.E. Goodson and H.-S. P. Wong, "Characterization of Phase-Change Layer Thermal Properties Using Micro-Thermal Stage," IEEE ITHERM Conference, pp. 744 – 749, Orlando, FL, May 27 – 30, 2014. DOI: 10.1109/ITHERM.2014.6892355
26. C. Ahn, S. Kim, T. Gokmen, O. Dial, M. Ritter, and H.-S. P. Wong, "Temperature-dependent Studies of the Electrical Properties and the Conduction Mechanism of

HfOx-based RRAM," *International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)*, Hsinchu, Taiwan, 28 – 30 April, 2014.

27. L. Zhao. H.-Y. Chen, S.-C. Wu, Z. Jiang, S. Yu, T.-H. Hou, H.-S. P. Wong, and Y. Nishi, "Improved Multi-level Control of RRAM Using Pulse-Train Programming," *International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)*, Hsinchu, Taiwan, 28 – 30 April, 2014. – best student paper award.
28. R. Liu, H.-Y. Chen, H. Li, P. Huang, L. Zhao, Z. Chen, F. Zhang, B. Chen, L. Liu, X. Liu, B. Gao, S. Yu, Y. Nishi, H.-S. P. Wong, and J. Kang, "Impact of Pulse Rise Time on Programming of Cross-Point RRAM Arrays," *International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)*, Hsinchu, Taiwan, 28 – 30 April, 2014.
29. Y. Wu, H. Yi, Z. Zhang, Z. Jiang, J. Sohn, S. Wong, H.-S. P. Wong, "First Demonstration of RRAM Patterned by Block Copolymer Self-Assembly," *IEEE International Electron Devices Meeting (IEDM)*, paper 20.8, December 9 – 11, Washington, D.C., 2013.
30. Y. Deng, H.-Y. Chen, B. Gao, S. Yu, S.-C. Wu, L. Zhao, B. Chen, Z. Jiang, T.-H. Hou, Y. Nishi, J.F. Kang, and H.-S. P. Wong, "Design and Optimization Methodology for 3D RRAM Arrays," *IEEE International Electron Devices Meeting (IEDM)*, paper 25.7, December 9 – 11, Washington, D.C., 2013.
31. S. Yu, H.-Y. Chen, Y. Deng, B. Gao, Z. Jiang, J. Kang, H.-S. P. Wong, "3D Vertical RRAM – Scaling Limit Analysis and Demonstration of 3D Array Operation," *Symp. VLSI Technology*, paper T11-4, pp. T158 – 159, Kyoto, Japan, June 11 – 14, 2013.
32. *J. Provine*, H.-S. P. Wong, S. S. Wong, S. Mitra, "Trusted Integrated Chips Integrating Non-Volatile Memory With CMOS," *38th Annual GOMACTech Conference*, Las Vegas, NV, March 11 – 14, 2013.
33. Y. Yang-Liauw, Z. Zhang, W. Kim, A. El-Gamal and S. Wong, "Nonvolatile 3D-FPGA with Monolithically Stacked RRAM-Based Configuration Memory," International Solid State Circuits Conference Digest of Technical Papers, pp. 406-407, San Francisco, CA, February 2012.
34. H.-Y. Chen, H. Tian, B. Gao, S. Yu, J. Liang, J. Kang, Y. Zhang, T.-L. Ren, H.-S. P. Wong, "Electrode/Oxide Interface Engineering by Inserting Single-Layer Graphene: Application for HfOx–Based Resistive Random Access Memory," *IEEE International Electron Devices Meeting (IEDM)*, paper 20.5, pp. 489 – 492, December 9 – 12, San Francisco, 2012.
35. H.-Y. Chen, S. Yu, B. Gao, P. Huang, J. Kang, and H.-S. P. Wong, "HfOx Based Vertical RRAM for Cost-Effective 3D Cross-Point Architecture without Cell Selector," *IEEE International Electron Devices Meeting (IEDM)*, paper 20.7, pp. 497 – 500, December 9 – 12, San Francisco, 2012.
36. S. Yu, *X. Guan*, and H.-S. P. Wong, "Understanding Metal Oxide RRAM Current Overshoot and Reliability Using Kinetic Monte Carlo Simulation," *IEEE International Electron Devices Meeting (IEDM)*, pp. 585 – 588, December 9 – 12, San Francisco, 2012.

37. J. Liang, S. Yeh, S. S. Wong, H.-S. P. Wong, “Scaling Challenges for the Cross-point Resistive Memory Array to Sub-10nm Node – An Interconnect Perspective,” *International Memory Workshop (IMW)*, Milan, Italy, pp. 61 – 64, May 20 – 23, 2012.

38. J. Chen, R.G.D. Jeyasingh, B. Gao, Y. Lu, Y.X. Deng, X.Y. Liu, J.F. Kang, H.-S. P. Wong, “Scaling Behavior of PCM Cells in Off-State Conduction,” *19th International Symposium on VLSI Technology, Systems and Applications (2012 VLSI-TSA)*, Hsinchu, Taiwan, 23- 25 April, 2012.