NMTRI Publications 2018

Journal Publications

1. Noriyuki Sato, Fen Xue, Robert M. White, Chong Bi, and Shan X. Wang, "Two-terminal spin–orbit torque magnetoresistive random access memory," Nature Electronics, 1(9): 508–511, 2018.
2. M. Lanza, H.-S. P. Wong, E. Pop, D. Ielmini, D. Strukov, B. C. Regan, L. Larcher, M. A. Villena, J. J. Yang, L.c Goux, A.o Belmonte, Y. Yang, F. M. Puglisi, J. Kang, B. Magyari-Köpe, E. Yalon, A. Kenyon, M. Buckwell, A. Mehonic, A. Shluger, H. Li, T.-H Hou, B.s Hudec, D.Akinwande, R. Ge, S. Ambrogio, J. B. Roldan, E. Miranda, J. Suñe, K. L. Pey, X. Wu, N. Raghavan, E. Wu, W. D. Lu, G. Navarro, W. Zhang, H. Wu, R. Li, A. Holleitner, U. Wurstbauer, M. C Lemme, M. Liu, S. Long, Q. Liu, H. Lv, A. Padovani, P. Pavan, I. Valov, X. Jing, T. Han, K. Zhu, S. Chen, F. Hui, Y. Shi, "Recommended methods to study resistive switching devices," Adv. Electronic Materials, vol. 5, issue 1, pages 1800143 (2018)
3. Y. Shi, X. Liang. B. Yuan, V. Chen. H. Li. F. Hui, Z. Yu, F. Yuan, E. Pop, H.-S. P. Wong, M. Lanza, "Electronic synapses made of layered two-dimensional materials," Nature Electronics, 1 (8), 458 (2018)
4. Z. Wang, S. Kumar, Yoshio Nishi and H.-S. P. Wong "Transient dynamics of NbOx threshold switches explained by Poole-Frenkel based thermal feedback mechanism", Applied Physics Letters, 112 (19), 193503, (2018).
5. Z. Wang, S. Kumar, H.-S. P. Wong and Yoshio Nishi, "Effect of Thermal Insulation on the Electrical Characteristics of NbOx Threshold Switches", Applied Physics Letters, 112.7 (2018)
6. S. Fujii, J.A. C. Incorvia, F. Yuan, S. Qin, F. Hui, Y. Shi, Y. Chai, M. Lanza, H.-S. P. Wong, "Scaling the CBRAM switching layer diameter to 30 nm improves cycling endurance," IEEE Electron Device Letters, 39 (1), 23-26 (2018).
7. Y. Shi, X. Liang, B. Yuan, V. Chen, H. Li, F. Hui, Z. Yu, F. Yuan, E. Pop, H.-S.P. Wong, M. Lanza, "Electronic Synapses Made of Layered Two-Dimensional Materials," Nature Electronics 1, 458-465 (2018)
8. E.C. Ahn, H.-S.P. Wong, E. Pop, "Carbon Nanomaterials for Non-Volatile Memories," Nat. Rev. Mater. 3, 18009 (2018)

Conference Publications

1. C.-H. Wang, C. McClellan, Y. Shi, X. Zheng, V. Chen, M. Lanza, E. Pop, and H.-S. P. Wong, "3D Monolithic Stacked 1T1R cells using Monolayer MoS_2 FET and hBN RRAM Fabricated at Low (150°C) Temperature," *International Electron Devices Meeting (IEDM)*, paper 22.5, December 1 – 5, San Francisco, 2018.
2. X. Zheng, R. Zarcone, D. Paiton, J. Sohn, W. Wan, B. Olshausen, and H.-S. P. Wong, "Error-Resilient Analog Image Storage and Compression with Analog-Valued RRAM Arrays: An Adaptive Joint Source-Channel Coding Approach," *International Electron Devices Meeting (IEDM)*, paper 3.5, December 1 – 5, San Francisco, 2018.
3. S. Deshmukh, C. Koroglu, M. Muñoz Rojo, S. Vaziri, E. Yalon, E. Pop, "Thermal Measurement of Resistive Memory (RRAM) Devices by Calibrated Scanning Thermal

Microscopy," Eurotherm Nanoscale & Microscale Heat Transfer VI (NMHT), Dec 2018, Levi, Finland

4. S. Deshmukh, R. Islam, C. Saltonstall, E. Yalon, T.E. Beechem, K.C. Saraswat, E. Pop, "Tuning Thermal and Electrical Properties of NiOx Films by UV/O3 Treatment for Resistive Memory Applications," MRS Fall Meeting, Nov 2018, Boston MA
5. K.L. Okabe, A. Sood, E. Yalon, C.M. Neumann, E. Pop, M. Asheghi, K.E. Goodson, H.-S.P. Wong, "Electrical and Thermal Analysis of Interfacial Phase Change Memory," E\PCOS (European Phase-Change and Ovonics Symposium), Catania Italy, Sep 2018 (Best Presentation Award, 3rd place)
6. E. Yalon, K. Okabe, C.M. Neumann, H.-S.P. Wong, E. Pop, "Improving PCM Energy-Efficiency by Reducing Pulse Widths," E\PCOS (European Phase-Change and Ovonics Symposium), Catania Italy, Sep 2018
7. S. Deshmukh, M. Muñoz Rojo, E. Yalon, S. Vaziri, E. Pop, "Nanoscale Thermometry of RRAM Filaments with Intimate Graphene Contacts," SRC TECHCON, Sep 2018, Austin, TX
8. C. Bi, N. Sato, R. Cheaito, R. M. White, M. Asheghi, K. E. Goodson and S. X. Wang, "Ultrafast 3-Terminal and 2-Terminal MRAM enabled by Spin-Orbit Torque or Thermally Assisted Switching", 2018 IEEE Magnetic Recording Conference (TMRC), Western Digital Milpitas Campus. August 9, 2018.
9. E. Yalon, K. Okabe, C.M. Neumann, H.-S.P. Wong, E. Pop, "Energy-Efficient Phase Change Memory Programming by Nanosecond Pulses," IEEE Device Research Conference (DRC), Jun 2018, Santa Barbara CA
10. S. Deshmukh, M. Muñoz Rojo, E. Yalon, S. Vaziri, E. Pop, "Probing Self-Heating in RRAM Devices by Sub-100 nm Spatially Resolved Thermometry," IEEE Device Research Conference (DRC), Jun 2018, Santa Barbara CA
11. Z. Jiang, S. Qin, H. Li, S. Fujii, D. Lee, S. Wong, H.-S. P. Wong, "Selector Requirements for Tera-Bit Ultra-High-Density 3D Vertical RRAM," Symp. VLSI Technology, Honolulu, HI, paper T10-3, June 18 – 22, 2018.
12. Y. Liao, H. Wu, W. Wan, W. Zhang, B. Gao, H.-S. P. Wong, and H. Qian "Novel In-Memory Matrix-Matrix Multiplication with Resistive Cross-Point Arrays," Symp. VLSI Technology, Honolulu, HI, paper T3-4, June 18 – 22, 2018