

NMTRI Publication and Presentations (up to 2011)

Refereed journal publications

1. E. Ou S. Wong, "Array Architecture for a Nonvolatile 3-Dimensional Cross-Point Resistance-Change Memory," to be published in *IEEE Journal of Solid State Circuits*, 2011.
2. B. Magyari-Köpe, S. Park, H. Lee, and Y. Nishi, "Understanding the switching mechanism in RRAM devices and the dielectric breakdown of ultrathin high-k gate stacks from first principles calculations", *ECS Transactions - ULSI vs. TFT*", 37, 2011.
3. C. Ahn, B. Lee, R.G.D. Jeyasingh, M. Asheghi, G.A.M. Hurkx, K.E. Goodson, H.-S. P. Wong, "Crystallization Properties and Their Drift Dependence in Phase-Change Memory Studied with a Micro-Thermal Stage," *J. Appl. Phys.*, 110, pp. 114520-1 – 114520-6 (2011).
4. S.Y. Wu, Y. Chai, H.-Y. Chen, S. Yu, H.-S. P. Wong, "Resistive Switching AlOx-Based Memory with CNT Electrode for Ultra-Low Switching Current and High Density Memory Application," *Symp. VLSI Technology*, paper 2B-3, Kyoto, Japan, June 13 – 16, 2011.
5. S. Yu, X. Guan, H.-S. P. Wong, "Conduction Mechanism of TiN/HfOx/Pt Resistive Switching Memory: A Trap-Assisted-Tunneling Model," *Applied Physics Letters*, vol. 99, pp. 063507-1 – 063507-3, 2011.
6. S. Yu, Y. Wu, H.-S. P. Wong, "Investigating the Switching Dynamics and Multilevel Capability in Bipolar Metal Oxide Resistive Switching Memory," *Applied Physics Letters*, 98, 103514, 2011.
7. S. Yu, Y. Wu, H.-S. P. Wong, "Investigating the Switching Dynamics and Multilevel Capability in Bipolar Metal Oxide Resistive Switching Memory," *Applied Physics Letters*, 98, 103514, 2011.
8. S. Yu, H.-S. P. Wong, "Compact Modeling of Conducting Bridge Random Access Memory (CBRAM)," *IEEE Trans. Electron Devices*, Vol. 58, No. 5, pp. 1352 - 1360, 2011.
9. S. Meister, S. Kim, J. Cha, H.-S. P. Wong, Y. Cui, "In Situ Transmission Electron Microscopy Observation of Nanostructural Changes in Phase-Change Memory," *ACS Nano*, vol. 5, no. 4, pp. 2742–2748, March 2011.
10. S. Kim, B. Lee, M. Asheghi, G.A.M. Hurkx, J. Reifenberg, K. Goodson, H.-S. P. Wong, "Resistance and Threshold Switching Voltage Drift Behavior in Phase-Change Memory and Their Temperature Dependence at Microsecond Time Scales Studied Using a Micro-Thermal Stage," *IEEE Trans. Electron Devices*, Vol. 58, No. 3, pp. 582 – 592, 2011.
11. Y. Nishi, "Nanoelectronic Devices and Integrations on Silicon Platform Today and Tomorrow", MINATEC Seminar, September, 2011, Grenoble, France
12. S. Kim, B.J. Bae, Y. Zhang, R.G. D. Jeyasingh, Y. Kim, I.-G. Baek, S. Park, S.-W. Nam, H.-S. P. Wong, "1D Thickness Scaling Study of Phase Change Material (Ge₂Sb₂Te₅) using a Pseudo 3-Terminal Device," *IEEE Trans. Electron Devices*, pp. 1483 – 1489, May, 2011

13. R.Y. Wang, M.A. Caldwell, R.G.D. Jeyasingh, S. Aloni, R.M. Shelby, H.-S.P. Wong, and D.J. Milliron, "Electronic and Optical Switching of Solution-Phase Deposited SnSe₂ Phase Change Memory Material," *J. Appl. Phys.* 109 (2011), 113506.
14. Y. Chai, Y. Wu, K. Takei, H.-Y. Chen, S. Yu, P.C.H. Chan, A. Javey, H.-S. P. Wong, "Nanoscale Bipolar and Complementary Resistive Switching Memory Based on Amorphous Carbon," *IEEE Trans. Electron Devices*, pp. 3933 – 3939, 2011.
15. Z. Li, J. Lee, J.P. Reifenberg, M. Asheghi, R.G.D. Jeyasingh, H.-S. P. Wong, K.E. Goodson, "Grain Boundaries, Phase Impurities, and Anisotropic Thermal Conduction in Phase-Change Memory," *IEEE Electron Device Letters*, Vol. 32, Issue 7, pp. 961 – 963 (2011).
16. R.G.D. Jeyasingh, D. Kuzum, and H.-S. P. Wong, "Investigation of Trap Spacing for the Amorphous State of Phase Change Memory Devices," *IEEE Trans. Electron Devices*, vol. 58, No. 12, pp. 4370 – 4376, 2011.
17. S. Yu, R. G. D. Jeyasingh, Y. Wu, H.-S. P. Wong, "AC Conductance Measurement and Analysis of the Conduction Processes in HfOx Based Resistive Switching Memory," *Applied Physics Letters*, 99, pp. 232105-1 – 232105-1 (2011); doi: 10.1063/1.366396.
18. Y. Wu, S. Yu, B. Lee, and H.-S. P. Wong, "Low-Power TiN/Al₂O₃/Pt Resistive Switching Device with Sub-20 μ A Switching Current and Gradual SET and RESET," *J. Applied Physics*, 110, pp. 094104-1 – 094104-5 (2011). <http://dx.doi.org/10.1063/1.3657938>
19. S. Park, B. Magyari-Köpe, and Y. Nishi, The impact of oxygen vacancies on the formation of a conductive channel in rutile TiO₂, *IEEE Electron Device Letters*, 32, 197, 2011
20. B. Magyari-Köpe, M. Tendulkar, S. Park, H. Lee, and Y. Nishi, "Resistive switching mechanisms in random access memory devices incorporating transition metal oxides: TiO₂, NiO and Pr_{0.7}Ca_{0.3}MnO₃", *Nanotechnology* 22, 254029, 2011
21. H.-S. P. Wong, S. Raoux, S. Kim, J. Liang, J.P. Reifenberg, B. Rajendran, M. Asheghi, K.E. Goodson, "Phase Change Memory," invited paper, *Proceedings of the IEEE*, Vol. 98, No. 12, pp. 2201 – 2227, December 2010
22. S. Yu, Y. Wu, H.-S. P. Wong, "Investigating the Switching Dynamics and Multilevel Capability in Bipolar Metal Oxide Resistive Switching Memory," *Applied Physics Letters*, 98, 103514, 2011
23. S. Kim, B.J. Bae, Y. Zhang, R.G. D. Jeyasingh, Y. Kim, I.-G. Baek, S. Park, S.-W. Nam, H.-S. P. Wong, "1D Thickness Scaling Study of Phase Change Material (Ge₂Sb₂Te₅) using a Pseudo 3-Terminal Device," *IEEE Trans. Electron Devices*, accepted for publication, 2011.
24. S. Meister, S. Kim, J. Cha, H.-S. P. Wong, Y. Cui, "In Situ Transmission Electron Microscopy Observation of Nanostructural Changes in Phase-Change Memory," *ACS Nano*, a vol. 5, no. 4, pp 2742–2748, March 2011
25. S. Yu, H.-S. P. Wong, "Compact Modeling of Conducting Bridge Random Access Memory (CBRAM)," *IEEE Trans. Electron Devices*, Vol. 58, No. 5, pp. 1352 - 1360, 2011
26. S. Kim, B. Lee, M. Asheghi, G.A.M. Hurkx, J. Reifenberg, K. Goodson, H.-S. P. Wong, "Resistance and Threshold Switching Voltage Drift Behavior in Phase-Change Memory

- and Their Temperature Dependence at Microsecond Time Scales Studied Using a Micro-Thermal Stage,” *IEEE Trans. Electron Devices*, Vol. 58, No. 3, pp. 582 – 592, 2011
27. S. Yu, H.-S. P. Wong, “A Phenomenological Model for the Reset Mechanism of Metal Oxide RRAM,” *IEEE Electron Device Letters*, vol. 31, No. 12, pp. 1455 – 1457, 2010. DOI: [10.1109/LED.2010.2078794](https://doi.org/10.1109/LED.2010.2078794)
 28. Y. Wu, B. Lee, H.-S. P. Wong, “Al₂O₃-based RRAM Using Atomic Layer Deposition (ALD) with 1 μ A Reset Current,” *IEEE Electron Device Letters*, vol. 31, No. 12, pp. 1449 – 1451, 2010. DOI: [10.1109/LED.2010.2074177](https://doi.org/10.1109/LED.2010.2074177)
 29. M. A. Caldwell, B. Haynor, S. Aloni, D. F. Ogletree, H.-S. P. Wong, J. J. Urban, and D. J. Milliron, “Spectroscopic Evidence for Exceptional Thermal Contribution to Electron Beam-Induced Fragmentation,” *J. Phys. Chem. C*, 2010, *114* (50), pp 22064–22068. DOI: [10.1021/jp1078086](https://doi.org/10.1021/jp1078086)
 30. S. Yu, J. Liang, Y. Wu, H.-S. P. Wong, “Read/Write Schemes Analysis for the Novel Complementary Resistive Switches in Passive Crossbar Memory Arrays,” *Nanotechnology*, vol. 21, pp. 465202, 2010. doi: [10.1088/0957-4484/21/46/465202](https://doi.org/10.1088/0957-4484/21/46/465202)
 31. J. Liang, H.-S. P. Wong, “Cross-Point Memory Array without Cell Selectors – Device Characteristics and Data Storage Pattern Dependencies,” *IEEE Trans. Electron Devices*, vol. 57, No. 10, pp. 2531-2538, 2010
 32. M. A. Caldwell, S. Raoux, R.Y. Wang, H.-S. P. Wong and D. J. Milliron, “Synthesis and size-dependent crystallization of colloidal germanium telluride nanoparticles,” *J. Mater. Chem.*, Volume 20, Issue 7, pp. 1285 – 1291 (2010). DOI: [10.1039/b917024c](https://doi.org/10.1039/b917024c)
 33. Hyung Dong Lee, Blanka Magyari-Kope, and Yoshio Nishi, "Model of Metallic Filament Formation and Rupture in NiO for Unipolar Switching", *Phys. Rev. B*, vol81, 2010, 193202
 34. Seong-Geon Park, Blanka Magyari-Kope, and Yoshio Nishi, "Electronic correlation effects in reduced rutile TiO₂ within the LDA+U method," *Phys Rev B* vol 81 (2010)
 35. M. Günhan Ertosun, K.-Y. Lim, C. Park, J. Oh, P. Kirsch and K. C. Saraswat, "Novel Capacitorless Single Transistor Charge Trap DRAM (1T 1C1T DRAM) Utilizing Electrons," *IEEE Electron Dev. Lett.*, Vol. 31, No. 5, May 2009, pp. 405-407.
 36. S. Raoux, H.-Y. Cheng, M. A. Caldwell, H.-S. P. Wong, “Crystallization Times of Ge-Te Phase Change Materials as a Function of Composition,” *Applied Physics Letters*, vol. 95, 07190-1 – 07190-3 (2009). DOI: [10.1063/1.3212732](https://doi.org/10.1063/1.3212732)
 37. Günhan Ertosun and Krishna C. Saraswat, "A Highly Scalable Capacitorless Double Gate Quantum Well Single Transistor DRAM" *IEEE Trans. Electron Dev.* Vol.57, No. 3, pp. 608-613, March 2010.
 38. W. Wang, S. Fujita and S. Wong, "Elimination of Forming Process for TiO_x Nonvolatile Memory Device," *IEEE Electron Device Letters*, Vol. 30, pp. 763-765, July 2009..
 39. W. Wang, S. Fujita and S. Wong, "RESET Mechanism of TiO_x Resistance-Change Memory Device," *IEEE Electron Device Letters*, Vol. 30, pp. 733-735, July 2009.
 40. Y. Zhang, S. Raoux, D. Krebs, L.E. Krupp, T. Topuria, M.A. Caldwell, D.J. Milliron, A. Kellock, P.M. Rice, J.L. Jordan-Sweet, H.-S. P. Wong, “Phase Change Nanodots Patterning Using a Self-Assembly Polymer Lithography and Crystallization Analysis”, *Journal of Applied Physics*, Vol.104, Issue 7, pp. 074312-1 074312-5, October 6, 2008. DOI: [10.1063/1.2981070](https://doi.org/10.1063/1.2981070)
 41. S. Meister, D. T. Schoen, M. A. Topinka, A. M. Minor, Y. Cui “Void Formation Induced Electrical Switching in Phase-Change Nanowires” *Nano Lett.* 8, 4562-4567 (2008).

42. S. Kim, Y. Zhang, J. McVittie, H. Jagannathan, Y. Nishi, H.-S. P. Wong, "Integrating Phase Change Memory Cell with Ge Nanowire Diode for Cross-Point Memory Experimental Demonstration and Analysis", *IEEE Trans. Electron Devices*, vol. 55, No. 9, pp. 2307-2313, September, 2008.
43. S. Verma, E. Pop, P. Kapur, K. Parat, and K. C. Saraswat, "Operational Voltage Reduction of Flash Memory Using High- κ Composite Tunnel Barriers," *IEEE Electron Dev. Lett.*, Vol. 29, No. 3, pp. 252-254, March 2008.
44. M. Gunhan Ertosun, H. Cho, P. Kapur, and K. C. Saraswat, "A Nanoscale Vertical Double-Gate Single-Transistor Capacitorless DRAM," *IEEE Electron Dev. Lett.*, Vol. 29, June 2008 pp. 615 – 617.
45. D. Milliron, M.A. Caldwell, H.-S. P. Wong, "Synthesis of Metal Chalcogenide Nanodot Arrays Using Block Copolymer-Derived Nanoreactors", *Nano Letters*, Vol. 7, No. 11, pp. 3503-3507 (2007) (DOI: [10.1021/nl072109b](https://doi.org/10.1021/nl072109b) September 28, 2007.)
46. S. Kim, H.-S. P. Wong, "Analysis of Temperature in Phase Change Memory Scaling", *IEEE Electron Device Letters*, vol. 2 Hoon Cho, Pawan Kapur, Pranav Kalavade and K. C. Saraswat, "Highly Scalable Vertical Double Gate NOR Flash Memory," Tech Digest of *IEEE IEDM*, Dec. 2007, pp. 917-920.
47. M. Günhan Ertosun, P. Kapur and K. C. Saraswat, "A Highly Scalable Capacitorless Double Gate Quantum Well Single Transistor DRAM: 1T-QW DRAM," *IEEE Electron Dev. Lett.*, Vol. 29, December 2008 pp. 1405-1407.
48. 8, No. 8, pp. 697-699, August, 2007.
49. J.R. Jameson, Y. Fukuzumi, Z. Wang, P. Griffin, K. Tsunoda, G.I. Meijer, and Y. Nishi, "Field-programmable rectification in rutile TiO₂ crystals," *Applied Physics Letters* 91, 112101 (2007) [3 pages]
50. Y. Zhang, H.-S. P. Wong, S. Raoux, J.N. Cha, C.T. Rettner, L.E. Krupp, T. Topuria, D.J. Milliron, P.M. Rice, J.L. Jordan-Sweet, "Phase Change Nanodot Arrays Fabricated Using a Self-Assembly Diblock Copolymer Approach", *Applied Physics Letters*, 91, 013104, July 2, 2007
51. Y. Chen and P.C. McIntyre, "Effects of Chemical Stability of Platinum/Lead Zirconate Titanate and Iridium Oxide/Lead Zirconate Titanate interfaces on Ferroelectric Thin Film Switching Reliability," *Appl. Phys. Lett.* 91, 232906-1-3 (2007).
52. Y. Chen and P.C. McIntyre, "Lead Zirconate Titanate Ferroelectric Thin Film Capacitors: Effects of Surface Treatments on Ferroelectric Properties," *Appl. Phys. Lett.* 91, 072910-1-3 (2007).
53. K. Tsunoda, Y. Fukuzumi, J.R. Jameson, Z. Wang, P.B. Griffin, and Y. Nishi, "Bipolar resistive switching in polycrystalline TiO₂ films," *Applied Physics Letters* 90, 113501 (2007) [3 pages].
54. J. Cha, Y. Zhang, H.-S. P. Wong, S. Raoux, C. Rettner, L. Krupp, V. Deline, Biomimetic Approaches for Fabricating High Density Nanopatterned Arrays, *Chemistry of Materials*, Vol. 19, pp. 839-843, February 20, 2007
55. Z. Wang, P. Griffin, J. McVittie, S. Wong, P. McIntyre and Y. Nishi, "Resistive Switching Mechanism in ZnX Cd_{1-X}S Nonvolatile Memory Devices," *IEEE Electron Device Letters*, Vol. 28, pp. 14-16, January 2007.
56. W. Wang, A. Gibby, Z. Wang, S. Fujita, K. Abe, P. Griffin, Y. Nishi, and S. Wong, "Non-volatile SRAM," *5th Semiconductor Memory Symposium*, Tokyo, Japan, January 2007

57. J.R. Jameson, P.B. Griffin, J.D. Plummer, and Y. Nishi, "Charge trapping in high-k gate stacks due to the bilayer structure itself," *IEEE Transactions on Electron Devices* 16 (53), 1858 (2006) [10 pages]
58. J.R. Jameson, W. Harrison, P.B. Griffin, J.D. Plummer, and Y. Nishi, "A semiclassical model of dielectric relaxation in glasses," *Journal of Applied Physics* 100 (12), 124104 (2006) [20 pages]

Invited talks

1. Y. Nishi, "RRAM, Challenges and Opportunities" Short Course at *International Memory Workshop*, May 22, 2011, Monterey, California
2. H.-S. P. Wong, S. Kim, B. Lee, M.A. Caldwell, J. Liang, Y. Wu, R.G.D. Jeyasingh, S. Yu, "Recent Progress of Phase Change Memory (PCM) and Resistive Switching Random Access Memory (RRAM)," invited paper, [International Memory Workshop](#), Monterey, CA, pp. 10 – 14, May 22 – 25, 2011.
3. H.-S. P. Wong, "Emerging Memory Devices," invited plenary paper, International Semiconductor Device Research Symposium (ISDRS), College Park, MD, December 7 – 9, 2011.
4. H.-S. P. Wong, "Emerging Memories: Are They Energy Efficient Enough?" invited paper, 2nd Annual Symposium on Energy Efficient Electronic Systems, Berkeley, CA, November 3 – 4, 2011.
5. H.-S. P. Wong, "Resistive Switching Memory (RRAM) - Modeling and Scaling Studies," keynote paper, First International Workshop on RRAM, September 20-21, 2011, Leuven, Belgium.
6. R. G. D. Jeyasingh, M.A. Caldwell, J. Liang, C. Ahn, H.-S. P. Wong, "Methodologies to Study the Scalability and Physics of Phase Change Memory Devices," European Phase Change and Ovonic Symposium (EPCOS), Zurich, Switzerland, September 4 – 6, 2011.
7. H.-S. P. Wong, S. Kim, B. Lee, M.A. Caldwell, J. Liang, Y. Wu, R.G.D. Jeyasingh, S. Yu, "Recent Progress of Phase Change Memory (PCM) and Resistive Switching Random Access Memory (RRAM)," invited paper, International Memory Workshop, Monterey, CA, pp. 10 – 14, May 22 – 25, 2011.
- 8.
9. Y. Nishi, "Materials Challenge of Integration of Nanoelectronic Devices and Circuits", *2010 Fall MRS Meeting*, Nanomaterials Integration for Electronics, Energy, and Sensing, Dec. 1-3, 2010 Boston, MA.
10. Y. Nishi, "VLSI Technologies, Past, Present and Future, challenges and opportunities" *Semicon Korea, Keynote address*, January 26, 2011, Seoul Korea
11. H.-S. P. Wong, S. Kim, M. A. Caldwell, J. Liang, R. Jeyasingh, "Scaling Studies of Phase Change Memory," Materials Research Society (MRS) Spring Meeting, R: Phase-Change Materials for Memory and Reconfigurable Electronics Applications, invited paper, paper R4.5, San Francisco, CA, April 25 – 28, 2011
12. M. Caldwell, D. Milliron, H.-S. P. Wong, "Challenges in Colloidal Phase Change Nanoparticle Devices," invited paper, European Phase Change and Ovonic Symposium (E*PCOS), Politecnico di Milano in Milano, Italy, September 6 – 7, 2010.

13. H.-S. P. Wong, S. Kim, B. Lee, M. Caldwell, J. Liang, Y. Wu, R. G. D. Jeyasingh, S. Yu, "Recent Progress of Phase Change Memory (PCM) and Resistance Change Memory (RRAM)," *10th International Conference on Solid State and Integrated Circuit Technology (ICSICT)*, Shanghai, China, November 1 – 4, 2010
14. M. Caldwell, S. Raoux, R. Y. Wang, D. Milliron, H.-S. P. Wong, "Synthesis and Electrical Characterization of Amorphous GeTe Nanoparticles," Materials Research Society (MRS) Spring Meeting, Symposium H: Phase-Change Materials for Memory and Reconfigurable Electronics Applications, invited paper, paper H4.5, San Francisco, CA, April 5 – 8, 2010
15. Y. Nishi, "Challenges and Opportunities for Future Nonvolatile Memory Technology", *2010 International Symposium on Next Generation Tera-bit- Memory Technology*, August 26, 2010 Hanyang University, Seoul, Korea
16. Y. Nishi, "Nonvolatile Memory Trend", *3rd Annual Meeting of International Collaborative R&D Project for Semiconductors*, Renaissance Hotel, Seoul, Korea, August 25, 2010
17. Y. Nishi, "Resistive Switching Mechanism and On-state Conduction", *Resistive Switch Memory Workshop*, April 4, 2010, Santa Clara Intel
18. J.R. Jameson and Yoshio Nishi, "The Roles of Oxygen Vacancies and Hydrogen Ions in TiO₂ Based Memory Devices:", *2010 ISIF*, Puerto Rico
19. Y. Nishi, H-S P. Wong and S. Wong, "Resistance Change Memory Materials and Devices, Mechanism and Scalability", *Nonvolatile Memory Technology Symposium*, October 26, 2009, Portland, OR
20. S. Kim, Y. Zhang, B. Lee, M. Caldwell, H.-S. P. Wong, "Fabrication and Characterization of Emerging Nanoscale Memory", *International Symposium on Circuits and Systems (ISCAS)*, Taipei, Taiwan, May 24-27, 2009.
21. Y. Zhang, S. Kim, B. Lee, M. Caldwell, H.-S. P. Wong, "Fabrication and Characterization of Emerging Nanoscale Memory", *International Disk Drive Equipment and Materials Association (IDEMA) Technical Symposium*, What's in Store for Storage, The Future of Non-Volatile Technologies, San Jose, CA, paper 5.3, December 11, 2008.
22. Y. Nishi, "Recent Progress in Resistance Change Memory" *American Vacuum Society Thin-films User Group meeting*, October 15, 2008, Santa Clara, CA
23. J.R. Jameson, "Hydrogen and TiO₂ resistance-change memory," *Monthly meeting of the Thin Film User Group, Northern California Chapter of the American Vacuum Society*, Santa Clara, CA, October 15, 2008
24. Y. Nishi, "Challenge of Nanoelectronic Materials and Devices toward New Nonvolatile Memories" *9th International Conference on Solid-State and Integrated-Circuit Technology*, October, 2008, Beijing, China
25. Y. Nishi and J.R. Jameson, "Recent progress in resistance change memory," *IEEE Device Research Conference (DRC)*, University of California, Santa Barbara, CA, June 23–25, 2008
26. Y. Nishi, "Challenges in Nanoelectronic Devices and Materials" *SPCC Conference*, April, 2008, Austin, TX
27. S. Raoux, C.T. Rettner, J. Jordan-Sweet, Y.-C. Chen, Y. Zhang, D. Milliron, M. Caldwell, J. Cha, and H.-S. P. Wong, "Scaling Properties of Phase Change Materials", *8th Annual Non-Volatile Memory Technology Symposium*, November 10-13, 2007, Albuquerque, New Mexico, U.S.A.

28. H.-S. P. Wong, "Emerging Memories", IEEE New Frontiers in Memory Symposium, San Jose, CA, September 20, 2007.
29. H.-S. P. Wong, "Emerging Memories", *7th International Workshop on Future Information Processing Technologies (IWFIPT)*, pp. 15, Dresden, Germany, 4-7 September 2007.
30. H.-S. P. Wong, "Phase Change Memory Modeling and Simulation", *Phase Change Memory Workshop*, Monterey, CA, August 26, 2007
31. P. McIntyre, **Y. Chen**, M. Kurasawa and R. Meyer, "Ferroelectric/Electrode Interface Layers: Their Effects on Reliable Ferroelectric Polarization Switching and Possible Resistance Switching," *Fall MRS Meeting*, Boston, MA, Nov. 27-Dec. 1, 2006.

Conference presentations

1. W Kim, S. Park, Z. Zhang, Y. Yang-Liau, D. Sekar, H.-S. P. Wong and S. Wong, "Forming Free Nitrogen-Doped AlOx RRAM with sub-uA Programming Current," *Symp VLSI Technology*, paper 2B-1, Kyoto, Japan June 2011.
2. S-G Park, B. Magyari-Köpe and Y. Nishi, "Theoretical Study of the Resistance Switching Mechanism in Rutile TiO_{2-x} for ReRAM," *Symp VLSI Technology*, paper 3B-2 Kyoto, Japan, June 2011.
3. Y. Wu, Y. Chai, H.-Y. Chen, S. Yu, H.-S. P. Wong, "Resistive Switching AlOx-Based Memory with CNT Electrode for Ultra-Low Switching Current and High Density Memory Application," *Symp. VLSI Technology*, paper 2B-3, Kyoto, Japan, June 13 – 16, 2011.
4. J. Liang, R. G.D. Jeyasingh, H.-Y. Chen, H.-S. P. Wong, "A 1.4 μ A Reset Current Phase Change Memory Cell with Integrated Carbon Nanotube Electrodes for Cross-Point Memory Application," *Symp. VLSI Technology*, paper 5B-4, Kyoto, Japan, June 13 – 16, 2011.
5. R.G.D. Jeyasingh, J.A.Chroboczek, G. Ghibaudo, M. Mouis, and H.-S. P. Wong "Low Frequency Noise in Phase Change Materials," *21st International Conference on Noise and Fluctuations (ICNF 2011)*, Toronto, Canada, June 12 – 16, 2011.
6. R.G.D. Jeyasingh, D. Kuzum, H.-S. P. Wong, "Direct measurement of trap spacing in phase change memory cells using ATE devices," *International Memory Workshop*, Monterey, CA, pp. 135 – 138, May 22 – 25, 2011.
7. S. Yu, Y. Wu, Y. Chai, J. Provine, H.-S. P. Wong, "Characterization of Switching Parameters and Multilevel Capability in HfOx/AlOx Bi-layer RRAM Devices," *18th International Symposium on VLSI Technology, Systems and Applications (2010 VLSI-TSA)*, pp. 106 – 107, Hsinchu, Taiwan, 25- 27 April, 2011.
8. B. Magyari-Köpe, and Y. Nishi, "Interface structures and band offsets in a model Ge-GeO_{2-x}-HfO₂-TiN metal gate stack: localization of oxygen vacancies near interfaces", *Materials Research Society (MRS) Spring Meeting*, San Francisco, USA, April 2011
9. Hyung Dong Lee, Blanka Magyari-Köpe, Kwanghee Cho and Yoshio Nishi, "Understanding of the resistive switching of unipolar NiO-based RRAM," *Materials Research Society (MRS) Spring Meeting*, San Francisco, USA, April 2011
10. Hyung Dong Lee, Seung Wook Ryu, Blanka Magyari-Köpe, Kwanghee Cho and Yoshio Nishi, "Reduction in reset current of unipolar NiO-based resistive switching through nickel interfacial layer", *Materials Research Society (MRS) Spring Meeting*, San Francisco, USA, April 2011.

11. Kwanghee Cho, Hyung Dong Lee, Seonggeon Park, Blanka Magyari-Köpe, Yoshio Nishi, Sungjoo Hong, Sungwoong Chung, Jinwon Park and Jaeyun Yi, "First principles study of the metal-oxide interfaces in Pt/TiO₂/Pt for resistive change memor" *Materials Research Society (MRS) Spring Meeting*, San Francisco, USA, April 2011
12. Kwanghee Cho, Hyung Dong Lee, Seonggeon Park, Blanka Magyari-Köpe, Yoshio Nishi, Sungjoo Hong, Sungwoong Chung, Jinwon Park and Jaeyun Yi, "Electronic structure study of the reduced anatase TiO_{2-x} using the GGA+Ud+Up method", *Materials Research Society (MRS) Spring Meeting*, San Francisco, USA, April 2011
13. B. Magyari-Köpe and Y. Nishi (invited), "Ab initio modeling of oxygen vacancies: understanding the switching mechanism in RRAM devices and the dielectric breakdown mechanism of ultrathin high-k based CMOS gate stacks", *SEMATECH*, Austin, TX, USA, March 2011
14. S. Yu, H.-S. P. Wong, "Modeling the Switching Dynamics of Programmable-Metallization-Cell (PMC) memory and Its Application as Synapse Device for a Neuromorphic Computation System," *IEEE International Electron Devices Meeting (IEDM)*, paper 22.1, pp. 520 – 523, December 6 – 8, San Francisco, 2010.
15. Y. Chai, Y. Wu, K. Takei, H.-Y. Chen, S. Yu, P.C.H. Chan, A. Javey, H.-S. P. Wong, "Resistive Switching of Carbon-Based RRAM with CNT Electrodes for Ultra-Dense Memory," *IEEE International Electron Devices Meeting (IEDM)*, paper 9.3, pp. 214 – 217, December 6 – 8, San Francisco, 2010.
16. J. Liang, W.-S. Jung, K. Saraswat, H.-S. P. Wong, "Low Temperature Vertical Polysilicon Diode Fabricated by Metal-Induced Lateral Crystallization (MILC) of Two Amorphous Silicon Layers with In-Situ Doping," *Materials Research Society (MRS) Fall Meeting*, paper G6.41, November 29 – December 3, Boston, MA, 2010.
17. Y. Wu, S. Yu, B. Lee, H.-S. P. Wong, "Gradual SET and RESET TiN/Al₂O₃/Pt resistive switching device with sub-20 μ A current," *Materials Research Society (MRS) Fall Meeting*, paper K4.2, November 29 – December 3, Boston, MA, 2010.
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